IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT: Behrens et al.

SERIAL No. Unassigned EXAMINER: Unassigned

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TITLE: DATA FLOW SYNCHRONIZATION

Attorney Docket No.: 20 01 0631

Commissioner For Patents
Washington, D.C. 20231

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Joanne A. Romaniello
Name

Joanne A Romaniello
Signature

PRELIMINARY AMENDMENT

Dear Sir:

Please amend the application as follows:

In The Abstract

Please amend the Abstract as follows:

A testing unit for testing a device under test (DUT) comprises a signal generator for applying a stimulus signal to the DUT, a receiving unit for receiving a response signal from the DUT on the applied stimulus signal, and a synchronizing unit for synchronizing a data flow of the response signal between the DUT and the receiving unit. The synchronizing unit receives a first clock signal (DUT-CLK) from the DUT and a second clock signal (CLK) from the testing unit. The synchronizing unit comprises a buffer for buffering data, a write unit for writing data from the DUT into the buffer, and a read unit for reading out data from the buffer to be provided to the receiving unit. A write access onto the buffer is controlled by the first clock signal (DUT-CLK), while a read access onto the buffer is controlled by

the second clock signal (CLK).

In The Claims

Please amend the claims as follows:

1. (Amended) A testing unit for testing a device under test (DUT), comprising:

a signal generator adapted for applying a stimulus signal to the DUT,

a receiving unit adapted for receiving a response signal from the DUT on the applied stimulus signal, and

a synchronizing unit for synchronizing a data flow of the response signal between the DUT and the receiving unit, whereby the synchronizing unit receives a first clock signal from the DUT and a second clock signal from the testing unit, the synchronizing unit including:

a buffer for buffering data,

a write unit for writing data from the DUT into the buffer, whereby a write access onto the buffer is controlled by the first clock signal, and

a read unit for reading out data from the buffer to be provided to the receiving unit, whereby a read access onto the buffer is controlled by the second clock signal.

2. (Amended) The testing unit of claim 1, wherein the buffer comprises a register structure with a plurality of registers.

3. (Amended) The testing unit of claim 2, further comprising:

a write pointer adapted to be moved between the pluralities of registers for defining one of the plurality of registers to receive and buffer data from the DUT, and

a read pointer adapted to be moved between the plurality of registers for

defining one of the pluralities of registers to be read out.

4. (Amended) The testing unit of claim 3, wherein the write pointer is adapted to be clocked by the first clock signal for successively writing successive data words from the DUT to different registers, and the read pointer is adapted to be clocked by the second clock signal for successively reading out successive data words buffered in the plurality of registers.

5. (Amended) The testing unit of claim 1, wherein the write unit comprises a latch controlled by the first clock signal, so that successive data words can be latched with the first clock signal and thus successively written into the buffer.

6. (Amended) The testing unit of claim 1, wherein the buffer is adapted to provide an initial delay time between a first valid write access and a first valid read access.

7. (Amended) The testing unit of claim 6, wherein the initial delay time is provided dependent on the maximum expected variation between such write and read accesses.

8. (Amended) A method for testing a device under test (DUT), the method comprising:

applying a stimulus signal to the DUT,

writing data in response to the stimulus signal from the DUT into a buffer, whereby a write access onto the buffer is controlled by a first clock signal of the DUT,

reading out data from the buffer to be provided to a receiving unit, whereby a read access onto the buffer is controlled by a second clock signal of the receiving unit, and

receiving the read out data in response to the stimulus signal by the receiving unit.

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9. (Amended) The method of claim 8, further comprising initializing a first valid write access and/or a first valid read access

Remarks

Claims 1-9 remain in the application.

The Abstract of the Disclosure has been amended to eliminate reference numbers.

Claims 1-9 have been amended to eliminate reference numbers and the phrase "the steps of." As such, claims 1-9 have been clarified by amendment for purposes of form. It is respectfully submitted that the amendments to claims 1-9 are neither narrowing nor made for substantial reasons related to patentablity as defined by the Court of Appeals for the Federal Circuit (CAFC) in Festo Corporation v. Shoketsu Kinzoku Kogyo Kabushiki Co., Ltd., 95-1066 (Fed. Cir. 2000). Therefore, the amendments to claims 1-9 do not create prosecution history estoppel and, as such, the doctrine of equivalents is available for all of the elements of claims 1-9.

Consideration and allowance of application is respectfully requested.

Attached hereto is a marked up version of the changes made to the abstract and claims by the current amendment. The attached page is captioned "Version With Markings to Show Changes Made."

Respectfully submitted,

10-26-01
Date

Paul D. Greeley
Attorney for Applicant(s)
Registration No. 31,019
Ohlandt, Greeley, Ruggiero & Perle, L.L.P.
One Landmark Square, 10th Floor
Stamford, CT 06901-2682
(203) 327-4500

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In The Abstract

Please amend the Abstract as follows:

A testing unit [(10)] for testing a device under test [–](DUT)[– (30)] comprises a signal generator [(20)] for applying a stimulus signal to the DUT [(30)], a receiving unit [(50)] for receiving a response signal from the DUT on the applied stimulus signal, and a synchronizing unit [(40)] for synchronizing a data flow of the response signal between the DUT [(30)] and the receiving unit [(50)]. The synchronizing unit [(40)] receives a first clock signal (DUT-CLK) from the DUT [(30)] and a second clock signal (CLK) [of] from the testing unit [(10)]. The synchronizing unit [(40)] comprises a buffer [(70)] for buffering data, a write unit [(80)] for writing data from the DUT [(30)] into the buffer [(70)], and a read unit [(90)] for reading out data from the buffer [(70)] to be provided to the receiving unit [(50)]. A write access onto the buffer [(70)] is controlled by the first clock signal (DUT-CLK), while a read access onto the buffer [(70)] is controlled by the second clock signal (CLK).

[[Fig. 1 for publication]]

In The Claims

Please amend the claims as follows:

1. (Amended) A testing unit [(10)] for testing a device under test [–](DUT)[– (30)], comprising:

a signal generator [(20)] adapted for applying a stimulus signal to the DUT [(30)],

a receiving unit [(50)] adapted for receiving a response signal from the DUT on the applied stimulus signal, and

a synchronizing unit [(40)] for synchronizing a data flow of the response

signal between the DUT [(30)] and the receiving unit [(50)], whereby the synchronizing unit [(40)] receives a first clock signal [(DUT-CLK)] from the DUT [(30)] and a second clock signal [(CLK) of] from the testing unit [(10)], the synchronizing unit [(40) comprising] including:

a buffer [(70)] for buffering data,

a write unit [(80)] for writing data from the DUT [(30)] into the buffer [(70)], whereby a write access onto the buffer [(70)] is controlled by the first clock signal [(DUT-CLK)], and

a read unit [(90)] for reading out data from the buffer [(70)] to be provided to the receiving unit [(50)], whereby a read access onto the buffer [(70)] is controlled by the second clock signal [(CLK)].

2. (Amended) The testing unit [(10)] of claim 1, wherein the buffer [(70)] comprises a register structure [(70)] with a plurality of registers [(70A-70H)].

3. (Amended) The testing unit [(10)] of claim 2, further comprising:

a write pointer [(100)] adapted to be moved between the pluralities of registers [(70A-70H)] for defining one of the plurality of registers [(70A-70H)] to receive and buffer data from the DUT [(30)], and

a read pointer [(110)] adapted to be moved between the plurality of registers [(70A-70H)] for defining one of the pluralities of registers [(70A-70H)] to be read out.

4. (Amended) The testing unit [(10)] of claim 3, wherein the write pointer [(100)] is adapted to be clocked by the first clock signal [(DUT-CLK)] for successively writing successive data words from the DUT [(30)] to different registers [(70A-70H)], and the read pointer [(110)] is adapted to be clocked by the second clock signal [(CLK)] for successively reading out successive data words buffered in the plurality of registers [(70A-70H)].

5. (Amended) The testing unit [(10)] of claim 1, wherein the write unit [(80)]

comprises a latch controlled by the first clock signal [(DUT-CLK)], so that successive data words can be latched with the first clock signal [(DUT-CLK)] and thus successively written into the buffer [(70)].

6. (Amended) The testing unit [(10)] of claim 1, wherein the buffer [(70)] is adapted to provide an initial delay time between a first valid write access and a first valid read access.

7. (Amended) The testing unit [(10)] of claim 6, wherein the initial delay time is provided dependent on the maximum expected variation between such write and read accesses.

8. (Amended) A method for testing a device under test [–](DUT)[– (30)], the method comprising [the steps of]:

[(a)] applying a stimulus signal to the DUT [(30)],

[(b)] writing data in response to the stimulus signal from the DUT [(30)] into a buffer [(70)], whereby a write access onto the buffer [(70)] is controlled by a first clock signal [(DUT-CLK)] of the DUT [(30)],

[(c)] reading out data from the buffer [(70)] to be provided to a receiving unit [(50)], whereby a read access onto the buffer [(70)] is controlled by a second clock signal [(CLK)] of the receiving unit [(50)], and

[(d)] receiving the read out data in response to the stimulus signal by the receiving unit [(50)].

9. (Amended) The method of claim 8, further comprising [a step of] initializing a first valid write access and/or a first valid read access.